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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/008,270
Filed: November 9, 2001
Inventor(s):
Carl Cavanagh, Carl B. Frankel, James P. Freyensee, and Steven A. Sivier

Title: Verification Simulator Agnosticity

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Examiner: Proctor, Jason Scott
Group/Art Unit: 2123
Atty. Dkt. No: 5181-96200

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal filed October 3, 2005, Appellants present this Appeal Brief. Appellant respectfully requests that this appeal be considered by the Board of Patent Appeals and Interferences.

I. REAL PARTY IN INTEREST

The present application is owned by Sun Microsystems, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at 4150 Network Circle, Santa Clara, CA 95054, as evidenced by the assignment recorded at Reel 012373, Frame 0838.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellant.

III. STATUS OF CLAIMS

Claims 1-6, 9-17, and 20-35 are pending. Claims 1-6, 9-17, and 20-35 are rejected under 35 U.S.C. § 103(a) and the rejection of these claims under section 103(a) is being appealed. A provisional rejection under the judicially-created doctrine of obviousness-type double patenting is currently being held in abeyance, and is not the subject of this appeal. A copy of claims 1-6, 9-17, and 20-35 is included in the Claims Appendix attached hereto.

IV. STATUS OF AMENDMENTS

No unentered amendment to the claims has been filed after final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a distributed simulation system (10, Fig. 1) comprising a first node (e.g. 12A) configured to simulate a first portion of a system under test (e.g. 20A) using a first simulator program (e.g. 46A) and a second node (e.g. 12B) configured to simulate a second portion of a system under test (e.g. 20B) using a second simulator program (e.g. 46B). The instruction code comprising the first simulator program differs from the instruction code comprising the second simulator program. The

first node and the second node communicate at least signal values during the simulation using message packets (100) formatted according to a grammar, and a simulation of the system under test comprises the first node simulating the first portion of the system under test and the second node simulating the second portion of the system under test. The distributed simulation system further comprises a hub (e.g. 12E) coupled to the first node and the second node, wherein the hub is configured to route the message packets from the first node to the second node and from the second node to the first node. (See, e.g., specification, page 5, lines 14-25; page 6, line 14-page 7, line 4; page 7, line 15-page 8, line 9; page 12, line 24-page 13, line 19).

Independent claim 12 is directed to a method. A first portion of a system under test (e.g. 20A) is simulated using a first simulator program (e.g. 46A) in a first node (e.g. 12A) of a distributed simulation system (10). A second portion of a system under test (e.g. 20B) is simulated using a second simulator program (e.g. 46B) in a second node (e.g. 12B) of the distributed simulation system. At least signal values are communicated during the simulating using message packets (100) formatted according to a grammar. The message packets are routed through a hub (e.g. 12E) coupled to the first node and the second node. The instruction code comprising the first simulator program differs from the instruction code comprising the second simulator program, and a simulation of the system under test comprises the first node simulating the first portion of the system under test and the second node simulating the second portion of the system under test. (See, e.g., specification, page 5, lines 14-25; page 6, line 14-page 7, line 4; page 7, line 15-page 8, line 9; page 12, line 24-page 13, line 19).

Independent claim 23 is directed to a computer readable medium (300) storing at least a first model (e.g. 20, Fig. 3) comprising a representation of logic to perform a non-blocking assignment and logic (56) to schedule a call of at least a first code sequence responsive to the non-blocking assignment, and the first code sequence comprising instructions executable to sample output signals and drive input signals of a second model (Fig. 11). (See, e.g., specification, page 14, line 26-page 15, line 20; page 24, line 15-page 31, line 11; page 45, line 23-page 46, line 12).

Independent claim 28 is directed to a computer readable medium (300) storing at least instructions executable to count timesteps in a distributed simulation system (10); and cause a cycle-based simulator (46D) to evaluate a clock cycle in a model (20D) responsive to a number of the timesteps equaling a number of timesteps per clock cycle of a clock corresponding to the model (See, e.g., Fig. 13 and specification, page 31, line 13-page 32, line 22).

Independent claim 30 is directed to a distributed simulation system (10) comprising a first node (e.g. 12A) configured to simulate a first portion of a system under test (e.g. 20A) using a first simulator program (e.g. 46A), a second node (e.g. 12B) configured to simulate a second portion of a system under test (e.g. 20B) using a second simulator program (e.g. 46B) and a hub (e.g. 12E) coupled to the first node and the second node, wherein the hub is configured to route message packets (100) from the first node to the second node and from the second node to the first node during simulation. The message packets include message packets that communicate at least signal values. The instruction code comprising the first simulator program differs from the instruction code comprising the second simulator program, and a simulation of the system under test comprises the first node simulating the first portion of the system under test and the second node simulating the second portion of the system under test. (See, e.g., specification, page 5, lines 14-25; page 6, line 14-page 7, line 4; page 7, line 15-page 8, line 9; page 12, line 24-page 13, line 19).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 12, and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Feinberg et al., U.S. Patent No. 5,910,903 ("Feinberg").

2. Claims 2-6, 13-17, 23-29, and 31-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Feinberg in view of "Handbook of Simulation" edited by Jerry Banks ("Banks").

3. Claims 9-11 and 20-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Feinberg in view of "Concepts of Programming Languages" by Robert Sebesta ("Sebesta").

4. Claims 1-6, 9-17, and 20-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Feinberg in view of Sano et al., U.S. Patent No. 5,991,533 ("Sano").

VII. ARGUMENT

First Ground of Rejection:

Claims 1, 12, and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Feinberg. Appellants traverse this rejection for at least the following reasons.

Claims 1, 12, and 30:

Appellant respectfully submits that each of claims 1, 12, and 30 recites a combination of features not taught or suggested in Feinberg. For example claim 1 recites a combination of features including: "a hub coupled to the first node and the second node, wherein the hub is configured to route the message packets from the first node to the second node and from the second node to the first node".

The Final Office Action mailed July 6, 2005 ("Final Office Action") alleges that the hub is taught by Feinberg's control computer (see Final Office Action, pages 10-11, item 2). Appellants respectfully disagree that Feinberg's control computer teaches the above recited hub. Feinberg teaches, with respect to Fig. 2, that "the present invention is overlaid onto the distributed simulation of Fig. 1 without disturbing how the distributed simulation of Fig. 1 operates" (Feinberg, col. 4, lines 26-28). With respect to Fig. 1, Feinberg teaches "The DIS software 110 on each simulation component 100 broadcasts Protocol Data Units ('PDUs') 120 to the DIS software 110 on each of the other simulation components 100. Each PDU 120 comprises information about the particular simulation entity 130 running on the simulation component 100 on which the DIS software 110 is resident so that each simulation component 100 may determine the relationship between each of the simulation entities 130" (Feinberg, col. 1, lines 59-67). Thus, Feinberg's

simulation components communicate PDUs directly with each other to perform a distributed simulation. Furthermore, Feinberg's teachings that his invention operates "in the background" (see, e.g., Feinberg, col. 7, lines 13-19) and "without disturbing how the distributed simulation operates" (see, e.g., Feinberg, col. 4, lines 27-28) teaches away from operating the control computer as a hub or inserting a hub.

Feinberg's control computer 200 collects data from the simulation components, observes the simulation for proper internal operation of models and proper interaction of models, analyzes simulation results, and enables optimization (Feinberg, col. 3, lines 41-45). Feinberg further teaches "the agent-applications 230 are programs designed to be sent to the simulators 100 to perform specific tasks such as gathering data from a simulator 100 regarding the resources of the simulator 100 or data provided to or generated by the simulation 130 resident on the simulator 100. Conversely, tools 240, 250 and 260 are designed to operate while resident on the control computer 200... the agent-applications monitor the simulation entity 130 and gather data relating to the simulation entity 130 such as what information input does the simulation entity 130 have (e.g., what information is in the PDUs that the simulation entity 130 is receiving or sending, how often are PDUs received/sent, etc.), or about the simulation component 100 system resources (e.g., what available random access memory, hard disk storage space, processing power, and/or communication bandwidth is available to the simulation component 100)...data gathered by the executing agent-applications 360 and/or pre-analyzed data as described above in step 420 is transmitted to the local control software 210 preferably to a data module 340 of the control software 210. Data module 340 may store the transmitted data in a database 350 for later use such as analysis by one or more of the tools 240, 250 or 260 or data module 340 may provide transmitted data directly to one or more of the tools 240, 250 and 260" (Feinberg, col. 5, lines 9-16 and 51-60; and col. 6, lines 12-20). Accordingly, Feinberg's control computer gathers data for analysis. Feinberg's control computer is not "a hub coupled to the first node and the second node, wherein the hub is configured to route the message packets from the first node to the second node and from the second node to the first node" as recited in claim 1.

The Final Office Action also includes a Response to Arguments section. The Response to Arguments section highlights the data gathering taught by Feinberg at col. 6, lines 12-20 as teaching data transmission in the direction of simulator to control computer (Final Office Action, page 3, second paragraph). The Response to Arguments section highlights the simulation control by Feinberg's control computer taught by Feinberg at col. 7, lines 19-25 as transmission in the direction of control computer to simulator (Final Office Action , page 3, third paragraph). The Response to Arguments section then concludes that Feinberg's control computer "is in communication with the simulators, receives data from the simulators for analysis, and in a preferred embodiment can control the simulators. Thus the control computer is indeed a hub in the distributed simulation taught by Feinberg." (Office Action, page 3, fourth paragraph). Appellants do not disagree that Feinberg's control computer is in communication with the simulators, receives data from the simulators for analysis, and can control the simulators. However, Appellants disagree that the control computer teaches "the hub is configured to route the message packets *from the first node to the second node* and *from the second node to the first node*".

Nothing in Feinberg's communication between the control computer and the simulators teaches or suggests a hub as recited in claim 1. Rather, Feinberg's control computer generates control commands and transmits them to the simulators, and collects data from the simulators. Thus, there is no communication from one simulator that is routed through the control computer to another simulator. Rather, communication between simulators is accomplished directly, by the PDUs exchanged directly between the simulators. Communication between the control computer and a given simulator is not routed to another simulator. In fact, Feinberg teaches away from using a hub as recited in claim 1, as highlighted above (that is, Feinberg teaches directly exchanging the PDUs between simulators and the control computer does not disturb this arrangement).

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 1 over Feinberg is in error and request reversal of the rejection. Claim 12 recites a combination of features including: "communicating at least signal values

during the simulating using message packets ... and routing the message packets through a hub coupled to the first node and the second node; ... wherein the first node and the second node communicate at least signal values during the simulating". The same teachings of Feinberg highlighted above are alleged to teach the above highlighted features of claim 12. Appellants respectfully submit that Feinberg does not teach or suggest the above highlighted features of claim 12, either. Claim 30 recites a combination of features including: "the hub is configured to route message packets from the first node to the second node and from the second node to the first node during simulation, the message packets including message packets that communicate at least signal values". The same teachings of Feinberg highlighted above are alleged to teach the above highlighted features of claim 30. Appellants respectfully submit that Feinberg does not teach or suggest the above highlighted features of claim 30, either. Accordingly, Appellants respectfully submit that the rejection of claims 12 and 30 is in error and request reversal of the rejection.

Second Ground of Rejection:

Claims 2-6, 13-17, 23-29, and 31-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Feinberg in view of Banks. Appellants traverse this rejection for at least the following reasons.

Appellants respectfully submit that Banks does not teach or suggest the combinations of features recited in claims 1 (on which claims 2-6 depend), 12 (on which claims 13-17 depend) and 30 (on which claims 31-35 depend), as highlighted above with regard to Feinberg. Accordingly, Appellants respectfully submit that the rejection of claims 2-6, 13-17, and 31-35 is in error for at least the reasons highlighted above with regard to claims 1, 12, and 30.

Claims 2, 13, and 31

Appellants respectfully submit that each of claims 2, 13, and 31 recite combinations of features not taught or suggested in Feinberg and Banks. Each of claims 2, 13, and 31 recite a combination of features including: "the first simulator program

comprises a first event-based simulator and the second simulator program comprises a second event-based simulator."

The Final Office Action notes that Feinberg does not teach event-based simulation, but asserts that Banks does teach event based simulation and that the motivation to use Banks' event-based simulation in Feinberg "would be found in the nature of the problem to be solved, such as the nature of the system for which the simulation is being designed, as well as the knowledge of ordinary skill in the art" (see Final Office Action, page 13, first paragraph). Appellants respectfully submit that the Final Office Action fails to form a *prima facie* case of obviousness of claims 2, 13, and 31 because a proper motivation to combine has not been established. Such a broad, conclusory statement as given in the Final Office Action does not meet the requirements of a *prima facie* case, in which particular findings of motivation must be set forth and substantial evidence must be provided (see, e.g., *In re Kotzab*, 55 USPQ2d, 1313, 1317 (Fed. Cir. 2000): "Whether the board relies on an express or an implicit showing, it must provide particular findings related thereto...broad conclusory statements alone are not 'evidence'").

In the Response to Arguments section, with regard to another claim, the Final Office Action states that the nature of the problem solved and the knowledge of ordinary skill in the art can be sources of a motivation to combine references. Appellants do not dispute this. However, it is still the burden of the Final Office Action to make particular findings of motivation and to provide substantial evidence to establish a *prima facie* case of obviousness. Thus, it is the Final Office Action's burden to explain in detail what the motivation to combine is, rather than merely stating its source, as the Final Office Action does.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 2, 13, and 31 over Feinberg and Banks is in error and request reversal of the rejection.

Claims 3, 14, and 32

Claims 3, 14, and 32 depend from claims 2, 13, and 31, respectively. Accordingly, the rejection of claims 3, 14, and 32 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that each of claims 3, 14, and 32 recite combinations of features not taught or suggested in Feinberg and Banks. For example, each of claims 3, 14, and 32 recite a combination of features including: "the first event-based simulator includes a first event scheduler which differs from a second event scheduler included in the second event-based simulator".

The Final Office Action alleges that the above highlighted features would be obvious in view of the fact that the simulators in Feinberg execute on different operating systems, which would have different process schedulers (see Final Office Action, page 13, second paragraph). Appellants respectfully submit that the process schedulers in the operating systems have nothing to do with event schedulers in simulators. Rather, the simulators would be a process or processes executing on the operating system, and would be scheduled with respect to other processes executing on the operating system. The operating system's scheduling of the simulators for execution has nothing to do with the internal processing of the simulators.

Furthermore, the Final Office Action asserts that "It would have been obvious...to use different schedulers for different event-based simulations in order to uphold principles well known in the art, such as those found in the handbook of simulation. Therefore it would have been obvious to build the distributed simulation system as taught by Feinberg, using event-based simulations with the particular scheduler that accurately represents the real system and therefore adheres to the principle of validation as taught by Banks." (Final Office Action, page 13, last paragraph continuing to page 14). Appellants respectfully submit that there is no support for the above reasoning in the art, nor in anything else that Appellants are aware of.

Still further, the rejection of claims 3, 14, and 32 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with

regard to claims 2, 13, and 31. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 3, 14, and 32 over Feinberg and Banks is in error and request reversal of the rejection.

Claims 4, 15, and 33

Claims 4, 15, and 33 depend from claims 2, 13, and 31, respectively. Accordingly, the rejection of claims 4, 15, and 33 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that each of claims 4, 15, and 33 recite combinations of features not taught or suggested in Feinberg and Banks. For example, each of claims 4 and 33 recite a combination of features including: "the first node further includes a model comprising a representation of logic to perform one or more non-blocking assignments and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment." Claim 15 recites a combination of features including: "scheduling a call of at least a first code sequence responsive to performing the non-blocking assignment".

The Final Office Action alleges that it would be obvious to incorporate non-blocking assignments into a simulation, referring to Appellants specification discussing such assignments as part of the IEEE 1394 standard and also referring to Bank's teachings regarding validation (see Final Office Action, page 14, second paragraph continuing to page 15). Appellants respectfully submit that even if, *arguendo*, the analysis in the Office Action is correct and incorporating non-blocking assignments into the simulation would be obvious, that still would not teach or suggest "a model comprising ... logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment".

Still further, the rejection of claims 4, 15, and 33 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with regard to claims 2, 13, and 31. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 4, 15, and 33 over Feinberg and Banks is in error and request reversal of the rejection.

Claims 5, 16, and 34

Claims 5, 16, and 34 depend from claims 1, 12, and 30, respectively. Accordingly, the rejection of claims 5, 16, and 34 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that each of claims 5, 16, and 34 recite combinations of features not taught or suggested in Feinberg and Banks. For example, each of claims 5, 16, and 34 recite a combination of features including: "the first simulator program comprises an event-based simulator and the second simulator program comprises a cycle-based simulator."

The Final Office Action alleges that Banks teaches a cycle-based simulator, stating "Activity scanning is regulated by time increments, and thus is cycle-based" (see Final Office Action, page 15, first full paragraph). Appellants respectfully disagree. Banks teaches that "Activity scanning produces a simulation program composed of independent modules waiting to be executed. Scanning takes place at fixed time increments at which a determination is made concerning whether or not an event occurs at that time. If an event occurs, the system state is updated." (Banks, page 9, section 1.4.3). Banks' scanning at fixed time increments to determine if an event occurs and optionally updating system state has noting to do with a cycle-based simulator. Rather, this description appears to be a different form of event-based simulation.

Still further, the rejection of claims 5, 16, and 34 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with regard to claims 2, 13, and 31. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 5, 16, and 34 over Feinberg and Banks is in error and request reversal of the rejection.

Claims 6, 17, and 35

Claims 6, 17, and 35 depend from claims 5, 16, and 34, respectively. Accordingly, the rejection of claims 6, 17, and 35 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that each of claims 6, 17, and 35

recite combinations of features not taught or suggested in Feinberg and Banks. For example, each of claims 6 and 35 recite a combination of features including: "the second node is configured to count a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator and to cause the cycle-based simulator to evaluate in response thereto". Claim 17 recites a combination of features including: "counting a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator in the second node; and causing the cycle-based simulator to evaluate in response to counting the number of timesteps."

The Final Office Action does not explicitly treat the features of claims 6, 17, and 35, grouping them with claims 5, 16, and 34, respectively. However, Appellants respectfully submit that even if, *arguendo*, the combination of Feinberg and Banks did teach the combinations of features recited in claims 5, 16, and 34, that would still not teach or suggest the above highlighted features of claims 6, 17, and 35.

Still further, the rejection of claims 6, 17, and 35 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with regard to claims 2, 13, and 31. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 6, 17, and 35 over Feinberg and Banks is in error and request reversal of the rejection.

Claim 23

Appellants respectfully submit that claim 23 recites a combination of features not taught or suggested in Feinberg and Banks. For example, claim 23 recites a combination of features including: "a first model comprising a representation of logic to perform a non-blocking assignment and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment, and the first code sequence comprising instructions executable to sample output signals and drive input signals of a second model".

The Final Office Action alleges that it would be obvious to incorporate non-blocking assignments into a simulation, referring to Appellants specification discussing such assignments as part of the IEEE 1394 standard and also referring to Bank's teachings regarding validation (see Office Action, page 16, second paragraph). Appellants respectfully submit that even if, *arguendo*, the analysis in the Office Action is correct and incorporating non-blocking assignments into the simulation would be obvious, that still would not teach or suggest "a first model comprising ... logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment". Furthermore, the above reasoning from the Final Office Action would not teach or suggest "the first code sequence comprising instructions executable to sample output signals and drive input signals of a second model" as recited in claim 23.

In the Response to Arguments section, the Office Action summarizes Appellants remarks by asserting "Applicants allege that it would not be obvious, in view of the cited references, to simulate a standards-compliant device in accordance with the particular standard (by referring to the standards compliant logic recited in the claim)" (Final Office Action, page 4, last paragraph continuing onto page 5). Appellants respectfully submit that this is an oversimplification of Appellants remarks and misses the point of the remarks. Appellants argue that the action taken in response to a non-blocking assignment would not be obvious. For example, claim 23 recites a combination of features including "*a first model* comprising a representation of logic to perform a non-blocking assignment and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment, and the first code sequence comprising instructions executable to sample output signals and drive input signals of *a second model*".

Thus, claim 23 recites a specific mechanism for responding to a non-blocking assignment (logic in the first model scheduling a call of at least a first code sequence responsive to the non-blocking assignment, and the first code sequence sampling output signals and drive input signals of a second model). The mere existence of non-blocking assignments in the prior art does not teach or suggest the above highlighted features in response to a non-blocking assignment. The Final Office Action has presented no

evidence that either Feinberg, Banks, or the IEEE 1394 standard teaches "a first model comprising a representation of logic to perform a non-blocking assignment and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment, and the first code sequence comprising instructions executable to sample output signals and drive input signals of a second model". The mere teaching of non-blocking assignments is insufficient to teach these specific features. Nothing in Feinberg, Banks, nor the combination thereof teaches or suggest the above highlighted features.

Appellants also note that the Office Action fails to provide a proper *prima facie* case of obviousness of claim 23 because it fails to provide a proper motivation to combine and/or modify the references. The Office Action states that "motivation to do so would be found in the nature of the system for which the simulation is designed, as well as the knowledge of one of ordinary skill in the art" (Office Action, page 11, last sentence). Such a broad, conclusory statement does not meet the requirements of a *prima facie* case, in which particular findings of motivation must be set forth and substantial evidence must be provided (see, e.g., *In re Kotzab*, 55 USPQ2d, 1313, 1317 (Fed. Cir. 2000): "Whether the board relies on an express or an implicit showing, it must provide particular findings related thereto...broad conclusory statements alone are not 'evidence'"). Thus, it is the Office Action's burden to explain in detail what the motivation to combine is, rather than merely stating its source, as the Final Office Action does. Accordingly, Appellants assert that a *prima facie* case of obviousness has not been proven.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 23 over Feinberg and Banks is in error and request reversal of the rejection.

Claim 24

Claim 24 depends from claim 23. Accordingly, the rejection of claim 24 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that claim 24 recites a combination of features not taught or suggested in Feinberg and

Banks. For example, claim 24 recites a combination of features including: "the first code sequence further includes instructions executable to trigger the non-blocking assignment."

The Final Office Action fails to explicitly treat the above highlighted features. Appellants respectfully submit that neither Feinberg, Banks, nor the combination thereof teaches or suggests the above highlighted features of claim 24. Still further, the rejection of claim 24 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with regard to claim 23. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 24 over Feinberg and Banks is in error and request reversal of the rejection.

Claim 25

Claim 25 depends from claim 24. Accordingly, the rejection of claim 25 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that claim 25 recites a combination of features not taught or suggested in Feinberg and Banks. For example, claim 25 recites a combination of features including: "the first code sequence includes instructions executable to trigger the non-blocking assignment for sampling signals and to trigger the non-blocking assignment again for driving signals."

The Final Office Action fails to explicitly treat the above highlighted features. Appellants respectfully submit that neither Feinberg, Banks, nor the combination thereof teaches or suggests the above highlighted features of claim 25. Still further, the rejection of claim 25 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with regard to claim 23. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 25 over Feinberg and Banks is in error and request reversal of the rejection.

Claim 26

Claim 26 depends from claim 23. Accordingly, the rejection of claim 26 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit

that claim 26 recites a combination of features not taught or suggested in Feinberg and Banks. For example, claim 26 recites a combination of features including: "the first model further includes a representation of logic configured to schedule a call of the first code sequence responsive to a sample clock edge."

The Final Office Action fails to explicitly treat the above highlighted features. Appellants respectfully submit that neither Feinberg, Banks, nor the combination thereof teaches or suggests the above highlighted features of claim 26. Still further, the rejection of claim 26 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with regard to claim 23. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 26 over Feinberg and Banks is in error and request reversal of the rejection.

Claim 27

Claim 27 depends from claim 23. Accordingly, the rejection of claim 27 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that claim 27 recites a combination of features not taught or suggested in Feinberg and Banks. For example, claim 27 recites a combination of features including: " the first model further includes a representation of logic configured to schedule a call of the first code sequence responsive to a timestep transition."

The Final Office Action fails to explicitly treat the above highlighted features. Appellants respectfully submit that neither Feinberg, Banks, nor the combination thereof teaches or suggests the above highlighted features of claim 27. Still further, the rejection of claim 27 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with regard to claim 23. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 27 over Feinberg and Banks is in error and request reversal of the rejection.

Claim 28

Appellants respectfully submit that claim 28 recites a combination of features not

taught or suggested in Feinberg and Banks. For example, claim 28 recites a combination of features including: "count timesteps in a distributed simulation system; and cause a cycle-based simulator to evaluate a clock cycle in a model responsive to a number of the timesteps equaling a number of timesteps per clock cycle of a clock corresponding to the model".

The Final Office Action alleges that Banks teaches a cycle-based simulator, stating "Activity scanning is regulated by time increments, and thus is cycle-based". Appellants respectfully disagree. Banks teaches that "Activity scanning produces a simulation program composed of independent modules waiting to be executed. Scanning takes place at fixed time increments at which a determination is made concerning whether or not an event occurs at that time. If an event occurs, the system state is updated." (Banks, page 9, section 1.4.3). Banks' scanning at fixed time increments to determine if an event occurs and optionally updating system state has noting to do with a cycle-based simulator. Particularly, this scanning for events at fixed time intervals has nothing to do with causing "a cycle-based simulator to evaluate a clock cycle in a model".

Furthermore, even if, *arguendo*, Banks did teach cycle-based simulators in general, this would still not teach or suggest "count timesteps in a distributed simulation system; and cause a cycle-based simulator to evaluate a clock cycle in a model responsive to a number of the timesteps equaling a number of timesteps per clock cycle of a clock corresponding to the model". Neither Feinberg, nor Banks, nor the alleged combination thereof teaches or suggests the above combination of features. Still further, the *prima facie* case of obviousness of claim 28 has not been established because a proper motivation has not been set forth, as highlighted above with regard to claims 2 and 23.

In the Response to Arguments section, the Final Office Action states "where Applicant's claim recites 'cause a cycle-based simulator to evaluate a clock cycle in a model responsive to a number of the timesteps equaling a number of timesteps per clock cycle of a clock corresponding to the model', the Examiner has shown that Banks teaches: if a specified condition is met, a rule is fired, meaning that an action is taken. For clarity,

the Examiner has interpreted '[the number of the timesteps] equaling a number of timesteps per clock cycle of a clock corresponding to the model' as Banks' 'specified condition'" (Final Office Action, page 7, bottom two paragraphs).

Appellants respectfully submit that Banks' broad teaching of some amorphous "specified condition" fails to teach or suggest the specific features recited in claim 28 (i.e. "a number of timesteps per clock cycle of a clock corresponding to the model"). For a proper *prima facie* case of obviousness, the combination of references must teach each and every feature of the claim. In no way does the broad "specified condition" even remotely teach or suggest "a number of timesteps per clock cycle of a clock corresponding to the model".

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 28 over Feinberg and Banks is in error and request reversal of the rejection.

Claim 29

Claim 29 depends from claim 28. Accordingly, the rejection of claim 29 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that claim 29 recites a combination of features not taught or suggested in Feinberg and Banks. For example, claim 29 recites a combination of features including: "instructions executable to sample output signals of the model and drive input signals of the model".

The Final Office Action fails to explicitly treat the above highlighted features. Appellants respectfully submit that neither Feinberg, Banks, nor the combination thereof teaches or suggests the above highlighted features of claim 29 in combination. Still further, the rejection of claim 29 suffers from the same failure to provide an actual motivation to combine the references that was highlighted above with regard to claim 23. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 29 over Feinberg and Banks is in error and request reversal of the rejection.

Third Ground of Rejection:

Claims 9-11 and 20-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Feinberg in view of Sebesta. Appellants traverse this rejection for at least the following reasons.

Appellants respectfully submit that Sebesta does not teach or suggest the combinations of features recited in claims 1 (on which claims 9-11 depend) and 12 (on which claims 13-17 depend), as highlighted above with regard to Feinberg. Accordingly, Appellants respectfully submit that the rejection of claims 9-11 and 20-22 is in error for at least the reasons highlighted above with regard to claims 1 and 12.

Claims 9 and 20

Appellants respectfully submit that each of claims 9 and 20 recite combinations of features not taught or suggested in Feinberg and Sebesta. For example, each of claims 9 and 20 recite a combination of features including: "the grammar includes a first command defining one or more logical ports and one or more logical signals."

The Final Office Action takes Official Notice that the use of grammars in computer communication is well known, and cites Sebesta, chapter 3. Sebesta, chapter 3 appears to be a general description of grammars for computer languages. However, nothing in the general nature of grammars or in Sebesta, chapter 3 teaches or suggests the specific features of claims 9 and 20: "the grammar includes a first command defining one or more logical ports and one or more logical signals."

Furthermore, the Final Office Action again fails to form a proper *prima facie* case of obviousness because the Final Office Action fails to establish a proper motivation to combine. Instead, the Final Office Action merely states that the motivation for designing a grammar that enables the invention to function as intended would be found in the nature of the particular problem to be solved by the invention as well as the knowledge of one of ordinary skill in the art. (See Final Office Action, page 18, item 10). Such a broad,

conclusory statement as given in the Final Office Action does not meet the requirements of a *prima facie* case, in which particular findings of motivation must be set forth and substantial evidence must be provided (see, e.g., *In re Kotzab*, 55 USPQ2d, 1313, 1317 (Fed. Cir. 2000): "Whether the board relies on an express or an implicit showing, it must provide particular findings related thereto...broad conclusory statements alone are not 'evidence'"). It is the burden of the Final Office Action, to establish a *prima facie* case of obviousness, to explain in detail what the motivation to combine is, rather than merely stating its source, as the Final Office Action does.

For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 9 and 20 over Feinberg and Sebesta is in error and request reversal of the rejection.

Claims 10 and 21

Claims 10 and 21 depend from claims 9 and 20, respectively. Accordingly, the rejection of claims 10 and 21 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that each of claims 10 and 21 recite combinations of features not taught or suggested in Feinberg and Sebesta. For example, each of claims 10 and 21 recite a combination of features including: "the grammar includes a second command defining a mapping between the logical signals and physical signals of a model of each portion of the system under test."

The Final Office Action again fails to treat the specific features of claims 10 and 21, instead merely broadly stating that grammars are known. Nothing in the general nature of grammars or in Sebesta, chapter 3 teaches or suggests the specific features of claims 10 and 21, highlighted above. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 10 and 21 over Feinberg and Sebesta is in error and request reversal of the rejection.

Claims 11 and 22

Claims 11 and 22 depend from claims 9 and 20, respectively. Accordingly, the

rejection of claims 11 and 22 is in error for at least the reasons given above. Furthermore, Appellants respectfully submit that each of claims 11 and 22 recite combinations of features not taught or suggested in Feinberg and Sebesta. For example, each of claims 11 and 22 recite a combination of features including: "the grammar includes a third command defining a routing between the logical ports of the portions of the system under test."

The Final Office Action again fails to treat the specific features of claims 11 and 22, instead merely broadly stating that grammars are known. Nothing in the general nature of grammars or in Sebesta, chapter 3 teaches or suggests the specific features of claims 11 and 22, highlighted above. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 11 and 22 over Feinberg and Sebesta is in error and request reversal of the rejection.

Fourth Ground of Rejection:

Claims 1-6, 9-17, and 20-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Feinberg in view of Sano. Appellants traverse this rejection for at least the following reasons.

Claims 1-6, 9-17, and 20-35

The Final Office Action fails to treat each individual claim in the fourth ground of rejection. Rather, the Final Office Action asserts that Feinberg anticipates claims 1-29, and that the dependent claims recite details that would have been obvious to one of skill in the art. Appellants respectfully disagree, and refer to the various arguments presented above for reasons why claims 1-6, 9-17, and 20-35 distinguish over Feinberg.

Sano is relied on to teach an IEEE 1364-1995 verification system. Sano does not teach or suggest the various features of claims 1-6, 9-17, and 20-35 that Feinberg fails to teach, as highlighted above with regard to the other grounds of rejection. Accordingly, the combination of Feinberg and Sano fails to teach or suggest the combinations of features recited in claims 1-6, 9-17, and 20-35.

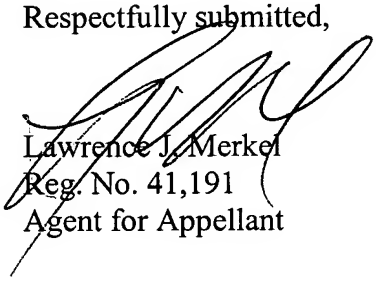
Furthermore, as with each other ground of rejection, the Final Office Action fails to prove a *prima facie* case of obviousness because a proper motivation to combine is not established. Instead, the Final Office Action merely states that the motivation would be found in the nature of the problem to be solved as well as the knowledge of one of ordinary skill in the art. Such a broad, conclusory statement as given in the Final Office Action does not meet the requirements of a *prima facie* case, in which particular findings of motivation must be set forth and substantial evidence must be provided (see, e.g., *In re Kotzab*, 55 USPQ2d, 1313, 1317 (Fed. Cir. 2000): "Whether the board relies on an express or an implicit showing, it must provide particular findings related thereto...broad conclusory statements alone are not 'evidence'"). It is the burden of the Final Office Action, to establish a *prima facie* case of obviousness, to explain in detail what the motivation to combine is, rather than merely stating its source, as the Final Office Action does.

VIII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-6, 9-17, and 20-35 under 35 U.S.C. § 103(a) was erroneous, and reversal of the decision is respectfully requested.

The Commissioner is authorized to charge the appeal brief fee of $500.00 and any other fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-96200/LJM. This Appeal Brief is submitted with a return receipt postcard.

Respectfully submitted,



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Date: November 10, 2005

IX. CLAIMS APPENDIX

The claims on appeal are as follows.

1. A distributed simulation system comprising:

a first node configured to simulate a first portion of a system under test using a first simulator program; and

a second node configured to simulate a second portion of a system under test using a second simulator program;

wherein the instruction code comprising the first simulator program differs from the instruction code comprising the second simulator program, and wherein the first node and the second node communicate at least signal values during the simulation using message packets formatted according to a grammar, and wherein a simulation of the system under test comprises the first node simulating the first portion of the system under test and the second node simulating the second portion of the system under test;

wherein the distributed simulation system further comprises a hub coupled to the first node and the second node, wherein the hub is configured to route the message packets from the first node to the second node and from the second node to the first node.

2. The distributed simulation system as recited in claim 1 wherein the first simulator program comprises a first event-based simulator and the second simulator program comprises a second event-based simulator.

3. The distributed simulation system as recited in claim 2 wherein the first event-based simulator includes a first event scheduler which differs from a second event scheduler included in the second event-based simulator.

4. The distributed simulation system as recited in claim 2 wherein the first node further includes a model comprising a representation of logic to perform one or more non-blocking assignments and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment.

5. The distributed simulation system as recited in claim 1 wherein the first simulator program comprises an event-based simulator and the second simulator program comprises a cycle-based simulator.

6. The distributed simulation system as recited in claim 5 wherein the second node is configured to count a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator and to cause the cycle-based simulator to evaluate in response thereto.

9. The distributed simulation system as recited in claim 1 wherein the grammar includes a first command defining one or more logical ports and one or more logical signals.

10. The distributed simulation system as recited in claim 9 wherein the grammar includes a second command defining a mapping between the logical signals and physical signals of a model of each portion of the system under test.

11. The distributed simulation system as recited in claim 9 wherein the grammar includes a third command defining a routing between the logical ports of the portions of the system under test.

12. A method comprising:

simulating a first portion of a system under test using a first simulator program in a first node of a distributed simulation system;

simulating a second portion of a system under test using a second simulator program in a second node of the distributed simulation system;

communicating at least signal values during the simulating using message packets formatted according to a grammar; and

routing the message packets through a hub coupled to the first node and the second node;

wherein the instruction code comprising the first simulator program differs from the instruction code comprising the second simulator program, and wherein the first node and the second node communicate at least signal values during the simulating using a grammar, and wherein a simulation of the system under test comprises the first node simulating the first portion of the system under test and the second node simulating the second portion of the system under test.

13. The method as recited in claim 12 wherein the first simulator program comprises a first event-based simulator and the second simulator program comprises a second event-based simulator.

14. The method as recited in claim 13 wherein the first event-based simulator includes a first event scheduler which differs from a second event scheduler included in the second event-based simulator.

15. The method as recited in claim 13 further comprising performing one or more non-blocking assignments in the first node; and scheduling a call of at least a first code sequence responsive to performing the non-blocking assignment.

16. The method as recited in claim 12 wherein the first simulator program comprises an event-based simulator and the second simulator program comprises a cycle-based simulator.

17. The method as recited in claim 16 further comprising:

counting a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator in the second node; and

causing the cycle-based simulator to evaluate in response to counting the number of timesteps.

20. The method as recited in claim 12 wherein the grammar includes a first command defining one or more logical ports and one or more logical signals.

21. The method as recited in claim 20 wherein the grammar includes a second command defining a mapping between the logical signals and physical signals of a model of each portion of the system under test.

22. The method as recited in claim 20 wherein the grammar includes a third command defining a routing between the logical ports of the portions of the system under test.

23. A computer readable medium storing at least:

a first model comprising a representation of logic to perform a non-blocking assignment and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment, and

the first code sequence comprising instructions executable to sample output signals and drive input signals of a second model.

24. The computer readable medium as recited in claim 23 wherein the first code sequence further includes instructions executable to trigger the non-blocking assignment.

25. The computer readable medium as recited in claim 24 wherein the first code sequence includes instructions executable to trigger the non-blocking assignment for sampling signals and to trigger the non-blocking assignment again for driving signals.

26. The computer readable medium as recited in claim 23 wherein the first model further includes a representation of logic configured to schedule a call of the first code sequence responsive to a sample clock edge.

27. The computer readable medium as recited in claim 23 wherein the first model further includes a representation of logic configured to schedule a call of the first code sequence responsive to a timestep transition.

28. A computer readable medium storing at least instructions executable to:

count timesteps in a distributed simulation system; and

cause a cycle-based simulator to evaluate a clock cycle in a model responsive to a number of the timesteps equaling a number of timesteps per clock cycle of a clock corresponding to the model.

29. The computer readable medium as recited in claim 28 further comprising instructions executable to sample output signals of the model and drive input signals of the model.

30. A distributed simulation system comprising:

a first node configured to simulate a first portion of a system under test using a first simulator program;

a second node configured to simulate a second portion of a system under test using a second simulator program; and

a hub coupled to the first node and the second node, wherein the hub is configured to route message packets from the first node to the second node and from the second node to the first node during simulation, the message packets including message packets that communicate at least signal values,

wherein the instruction code comprising the first simulator program differs from the instruction code comprising the second simulator program, and wherein a simulation of the system under test comprises the first node simulating the first portion of the system under test and the second node simulating the second portion of the system under test.

31. The distributed simulation system as recited in claim 30 wherein the first simulator program comprises a first event-based simulator and the second simulator program comprises a second event-based simulator.

32. The distributed simulation system as recited in claim 31 wherein the first event-based simulator includes a first event scheduler which differs from a second event scheduler included in the second event-based simulator.

33. The distributed simulation system as recited in claim 31 wherein the first node further includes a model comprising a representation of logic to perform one or more non-blocking assignments and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment.

34. The distributed simulation system as recited in claim 30 wherein the first simulator program comprises an event-based simulator and the second simulator program comprises a cycle-based simulator.

35. The distributed simulation system as recited in claim 34 wherein the second node is configured to count a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator and to cause the cycle-based

simulator to evaluate in response thereto.

X. EVIDENCE APPENDIX

No evidence submitted under 37 CFR §§ 1.130, 1.131 or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings known to Appellant.